Enhanced Boiling of a Dielectric Liquid on Copper Nanowire Surfaces

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ABSTRACT
Copper nanowire arrays on a silicon (Si) substrate were fabricated by electro-chemical deposition through an anodic aluminum oxide (AAO) template to generate a high performance boiling surface. In this study, the pitch (~300 nm) and diameter (~200 nm) of the nanowires were fixed, and the height was varied between 1 and 8 μm. It is observed that copper nanowire surfaces increase the critical heat flux and reduce the incipience superheat compared to the baseline experiments, which were performed using a plain surface without nanowires. The work reported here is a major enhancement over previous studies on structured surfaces, which mainly considered structures which were on the order of 100 μm.

Keywords: pool boiling, nucleate boiling, nanowire, AAO, boiling enhancement, efficient surface, heat transfer

NOMENCLATURE

q Heat flux [W/cm^2]
T_{sat} Saturation temperature [K]
T_w Wall temperature (Test surface temperature) [K]
T_∞ Bulk temperature [K]

Greek Symbols
ΔT_{sat} Wall superheat; T_w -T_{sat} [K]
ΔT_{sub} Liquid subcooling; T_{sat} - T_∞ [K]

1. INTRODUCTION

1.1 Background

Increasing heat fluxes in semiconductor devices are a direct result of larger transistor density, higher-speed processing, and more sophisticated functions being performed by the chips. Although there are many promising solutions to address this thermal management issue, boiling is a leading candidate due to the large heat transfer coefficients associated with liquid-vapor phase change, as well as, reducing thermal gradients in the chip compared to single-phase cooling. Considerable efforts have been made to enhance nucleate boiling heat transfer through surface modifications. Protrusions, re-entrant cavities, and porous structures have been investigated [1-9], with a focus on varying the length scales of these structures. These surface modifications increase the number of nucleation sites, the boiling surface area, and the rewetting performance. In doing so, they decrease the nucleate boiling incipience superheat and/or increase the critical heat flux (CHF).

In this study, copper nanowire arrays fabricated on a silicon substrate are used to enhance nucleate boiling performance. The nanowires increase the critical heat flux. In addition, the larger number of nucleation sites leads to higher heat transfer coefficients. Copper nanowires are highly conductive, are

effective at short heights, and can be integrated with future semiconductor cooling methodologies. For example, 3D stacked architectures require thermal solutions on the order of less than 100 μm. If a 100 μm diameter microchannel is considered, due to the small length scale of copper nanowires, they can be used to further increase the heat transfer in this microchannel without greatly increasing the pressure drop across the microchannel. This is an enhancement over previous studies [1-9] on structured surfaces, which mainly considered structures themselves on the order of 100 μm. Since, nucleate boiling is the dominant heat transfer mechanism for small-sized microchannels [10], enhancing nucleate boiling is an important area of study.

1.2 Enhanced nucleate boiling literature

An extensive review of micro-structured surfaces for boling enhancement is reported by Nakayama [11], Thome [12], and Webb [13]. These authors analyzed the effect of various surface geometries, such as low finned tube, Thermoexcel-E, High Flux, Gewa-T, Turbo-B, star insert, twisted tape, microfinned tube, and re-entrant channels, on the critical heat flux and heat transfer coefficient. These surfaces enhanced boiling by increasing the number of nucleation sites and increasing the liquid film contact area.

Recently, various protrusion, re-entrant cavity, and porous structures for boiling enhancement have been made by using Micro Electro Mechanical System (MEMS) technology. Honda et al. [1] studied protrusion structures by fabricating micro-pin fins with submicron-scale roughness to enhance boiling. Square pin-fins with dimensions of 50 x 50 x 60 μm^3 (width x thickness x height) and submicron-scale roughness (RMS roughness of 25 to 32 nm) were fabricated on the surface of square silicon chip (10 x 10 x 0.5 mm^3) by wet and dry etching respectively. Experimental results for degassed FC-72 revealed that the CHF (Critical Heat Flux) for this surface was 1.8 to 2.3 times that of smooth silicon. The results showed that nano-scale surface features can affect the nucleate boiling heat transfer. Other protrusion structures were investigated by Mitrovic and Hartmann [2]. The authors fabricated cylindrical copper rods by combining electrocoating and etching processes. The rods had diameters between 1 and 25 μm and heights ranging from 10 to 100 μm and were fabricated on the outside of a cylindrical test tube. Pool boiling experiments with refrigerant R141b showed a lower boiling incipient point and a doubling in the heat transfer coefficient. Carbon nanotubes (CNTs) have also been considered as protrusion boiling structures. Ujereh et al. [3] examined multi-walled nanotubes (MWNT) having a diameter of approximately 50 nm and a height ranging from 20 to 30 μm. These MWNTs were grown on a silicon surface with different array densities and area coverages. Fully coating the substrate surface with CNTs was highly effective, and the CHF was improved by 45% over smooth silicon surface. Ahn et al. [4] studied the effect of MWNTs with 8-15 nm diameters and two different heights (9 μm and 25 μm). For nucleate boiling of PF-5060, MWNTs yielded a 26 – 29 % higher CHF under saturated conditions compared to a bare silicon surface.

In addition to the previous protrusion structure studies, investigations have been conducted on using cavities structures for boiling enhancement. Yu et al. [5] fabricated cylindrical cavities on a 625 μm thick, 10 mm x 10 mm square silicon plate. The authors studied cavities with three different diameters (200, 100, 50 μm) and two different depths (200 and 110 μm). The pool boiling experiment in FC-72 showed that the maximum value of CHF for the cavity structures was almost 2.5 times that of the plain silicon surface. Nimkar et al. [6] studied the effect of micro-pyramidal re-entrant cavities with a 240 μm square base, a 40 μm square mouth, and a 140 μm depth. They studied cavities having different pitches of 0.5, 0.75, and 1.0 mm in FC-72. The authors' samples were positioned vertically, i.e. the samples were rotated 90˚ with respect to gravity. The boiling curve comparison showed that a surface with 0.75 mm pitch had the highest heat transfer augmentation and the highest active site density.

Finally, porous structures, the last type of boiling surface enhancement structures, were studied by Vemuri and Kim [7], who used anodized aluminum oxide (AAO) as a nano-porous surface. The diameter of the pores was between 50 and 250 nm. For pool boiling of saturated FC-72, there was a decrease of ~30% in the incipient superheat for the nano-porous coated surface compared to that of a plain surface. This result shows that a nano-sized pore can trap vapor, which results in a lower

superheat. Furthermore, You et al. [8] studied microporous coatings, which were a mixture of small particles (1 to 20 μm diameter) and an epoxy binder that creates a thin (about 50 μm), porous structure that contains re-entrant cavities. For pool boiling of FC-72, the CHF was almost 2 times that of the smooth copper surface. Finally, El-Genk and Parker [9] investigated enhanced boiling on porous graphite. The surface pores and re-entrant cavities in the porous graphite vary in size from a few to hundreds of μm. For pool boiling of HFE-7100 from these surfaces, the CHF was 40% higher than smooth copper.

The aforementioned methods show effective surfaces for nucleate boiling. Figure 1 shows a performance summary of various prior studies using protrusion, re-entrant cavity, and porous structures as a function of CHF and thickness. From the graph, longer structures lead to higher CHF values. However, it is difficult to effectively apply these technologies to microchannels below 100 μm hydraulic diameter because of their size.

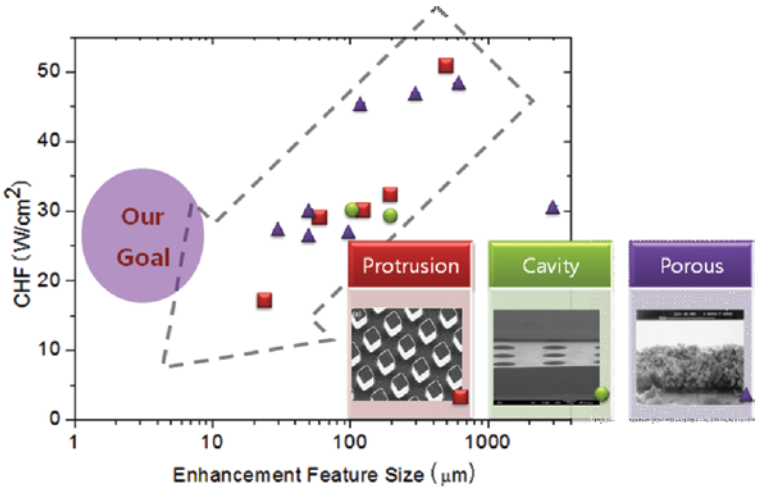


Figure 1. Effect of feature size on CHF for different surface enhancement techniques.

For microchannels used for cooling of 3D chip architectures, surface modifications need to be as thin as possible. In addition, a high thermal conductivity material should be used to minimize thermal conduction resistance. Also, since many applications may require two phase microchannel boiling, a thin and controllable nano structure is necessary for future technologies.

Currently, only a few studies have been made on creating thin surface modifications with copper for boiling enhancement. Li et al. [14] fabricated Cu nanorods having 50 nm diameter and 450 nm height using oblique-angle deposition. In a pool boiling experiment of water, the wall superheat was decreased, and the CHF was improved by about 10% compared to a flat Cu surface. The authors showed that multiple scales from nano to micro play a key role in enhancing the nucleate boiling performance. Chen et al. [15] synthesized Cu and Si nanowires by electroplating Cu into nanoscale pores and aqueous electroless etching (EE) techniques respectively. The pool boiling experiments with water showed more than 100% increase in the CHF value. The present work focuses on the effect of nanowire height on the pool boiling performance. The dielectric fluid PF-5060 is used instead of water, since many applications involving direct contact with an active chip may require this.

2. EXPERIMENTAL INVESTIGATION

Experiments are conducted to examine the effectiveness of copper nanowires attached to a silicon substrate with degassed PF-5060 under atmospheric, saturated boiling conditions. The boiling performance of the copper nanowire arrays is compared to an uncoated silicon surface and previously

published literature on enhanced surfaces. A thermal test assembly used in this study is shown in Figure 2. The thermal test assembly consists of three separate fabrication processes.

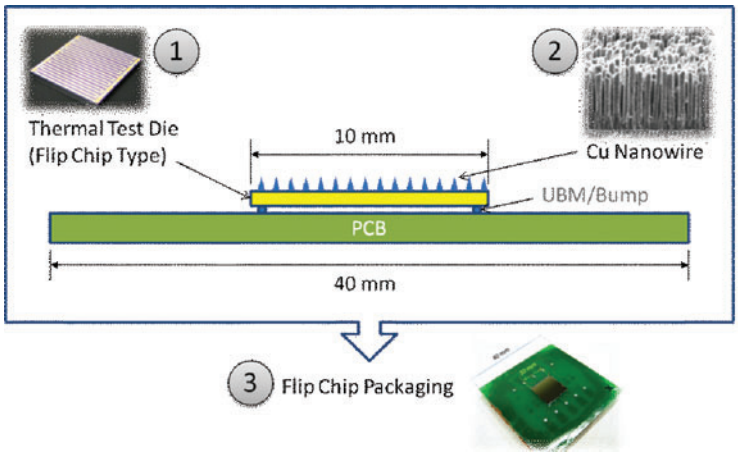


Figure 2. Thermal test assembly schematic showing the three parts of fabrication: thermal test die, copper nanowires, and packaging.

2.1 Test chip fabrication

The first fabrication process for the thermal test assembly was the fabrication of a thermal test chip. The thermal test chip consists of a platinum (Pt) resistive temperature device (RTD) patterned on one side of a silicon substrate. The RTD is used to provide a uniform and known heat flux to the fluid, while simultaneously providing an averaged surface temperature measurement.

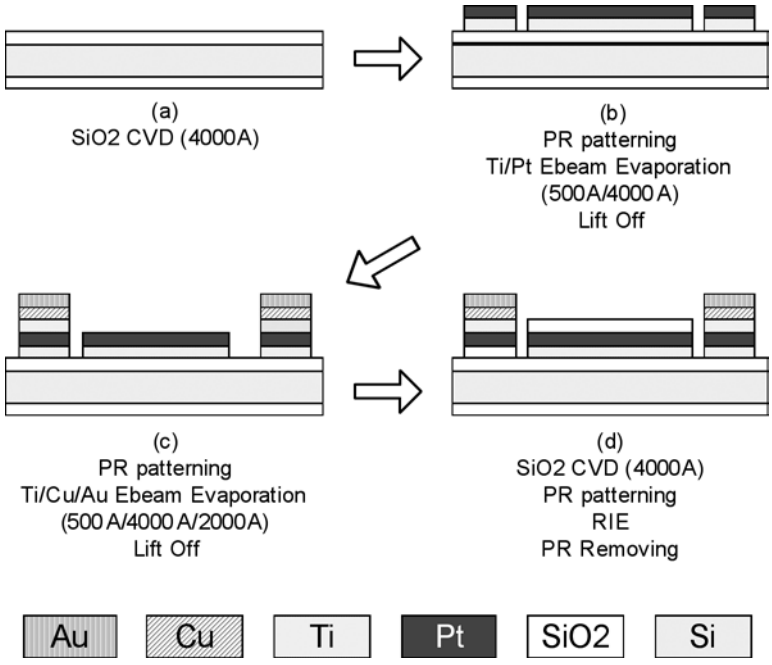


Figure 3. Thermal test chip fabrication process outline.

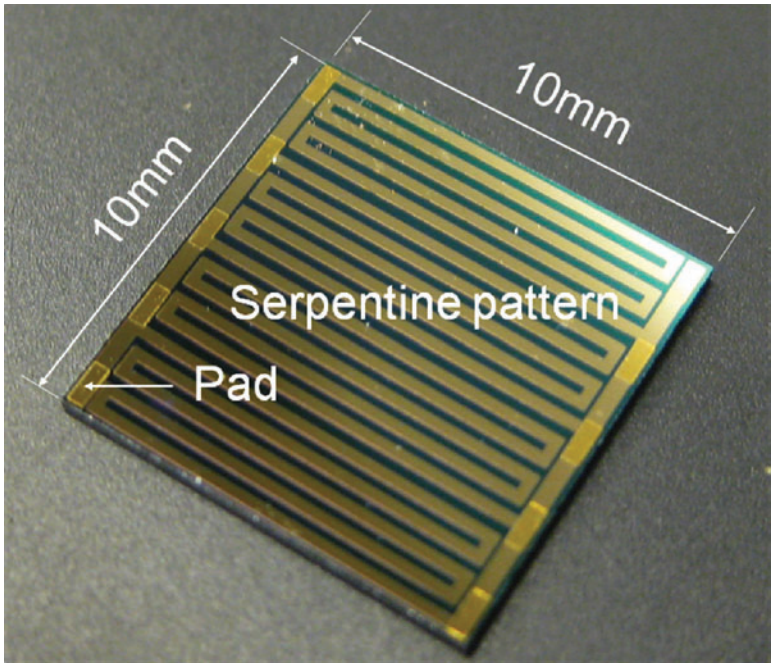


Figure 4. Thermal test chip Pt RTD pattern. The serpentine pattern provides uniform heating and an average surface temperature measurement. The contact pads are shown on the left and right sides of the device.

Figure 3 shows the two step lift-off process for fabricating the Pt RTD. Initially, as shown in Figure 3a, a Si wafer is covered with a silicon oxide (SiO_2) layer of 0.4 μm thickness by Plasma Enhanced Chemical Vapor Deposition (PECVD) to act as an electrical insulation layer. Negative photo resist, NR9-8000 (Futurex), is spun on the silicon wafer and sequentially developed to prepare the surface for lift-off patterning. Next, 0.05 μm of Titanium (Ti) and 0.4 μm of Pt are deposited by Ebeam (Electron beam) process on to the patterened NR9-8000. The Ti and Pt act as an adhesion layer and RTD layer respectively. Subsequently, the Ti/Pt layers are patterned with a lift-off process by using photoresist remover, RR-41 (Futurex) for 1h at 80°C. The resulting fabrication is shown in Figure 3b.

In order to electrically connect the Pt RTD on the silicon substrate to a packaging board, contact pads need to be formed on the RTD. The above lift-off process is repeated with a different pattern and different deposited metals to achieve this goal. 0.05 μm of Ti, 0.4 μm of Cu, and 0.2 μm of gold (Au) are deposited as an adhesion layer, solder wetting layer, and oxidation inhibiting layer respectively. This is seen in Figure 3c. Then, in order to provide electrical passivation of the RTD, a 0.4 μm thick SiO_2 layer is deposited by PECVD. Finally, the SiO_2 layer is selectively etched using Reactive Ion Etching (RIE) to open up the contact pads. The complete fabrication can be seen in Figure 3d, while a picture of thermal test chip is presented in Figure 4.

2.2 Fabrication of copper nanowires

Recently, template approaches to fabricate nanostructures have been studied extensively. Desired nanostructure geometry, coverage density, and properties can be fabricated by depositing various materials through a nanotemplate. Among the various templates with nanopores, AAO is used as the template for this study to fabricate regular and aligned nano wires of various lengths with an electrochemical deposition process. AAO with uniform and parallel porous structure is prepared by anodic oxidation of aluminum in an acidic electrolyte [16, 17]. AAO is the material of choice for the template electrochemical deposition because it is an electrical insulator, is chemically and thermally

inert, has good wetting property for electrolytes, is easy to release, and is easy to handle during experiments [18].

Figure 5 depicts an example of a nanowire array. This structure is fabricated by electrochemically assisted, template growth of copper. Commercial AAO samples (Anodisc 25, Whatman, 200 nm pore, 60 μm thick, 25 mm diameter) were used as the template. Ti, Cu, and Au thin films (50, 400, and 200 nm respectively) were deposited onto one side of template by Ebeam evaporation. These thin metal films served as adhesion, initialization, and oxide inhibition layers, respectively. The AAO sample was then attached to an electrode with the thin film deposition side in contact with the electrode.

Additionally, an electrolytic bath consisting of sulfuric acid (120mL/L), copper sulfate (90 g/L), a copper carrier (12 mL/L), and a copper additive (6 mL/L) was made in a 2 L glass beaker. Two Cu electrodes were placed in the electrolytic bath and were connected to a power supply. The electrochemical depositions were conducted at 2.5 mA/cm^2 DC at room temperature. Before starting any electrochemical depositions, the system was run for 30 minutes without the AAO sample in order to stabilize. Immediately following the stabilization period, the electrode with the AAO sample was placed in the electrolytic bath and the power supply was turned on. Varying the electrochemical deposition time generated various sample heights. A growth rate of 0.1 μm/min was found.

After the sample had been deposited with Cu, the AAO template was removed from the electrode and attached to the silicon test chip by using Ag-filled epoxy, ablebond 2000T (Ablestik). Finally, the copper nanowires were released from the AAO by dissolving the AAO template in 5 wt% NaOH solution for 5 min.

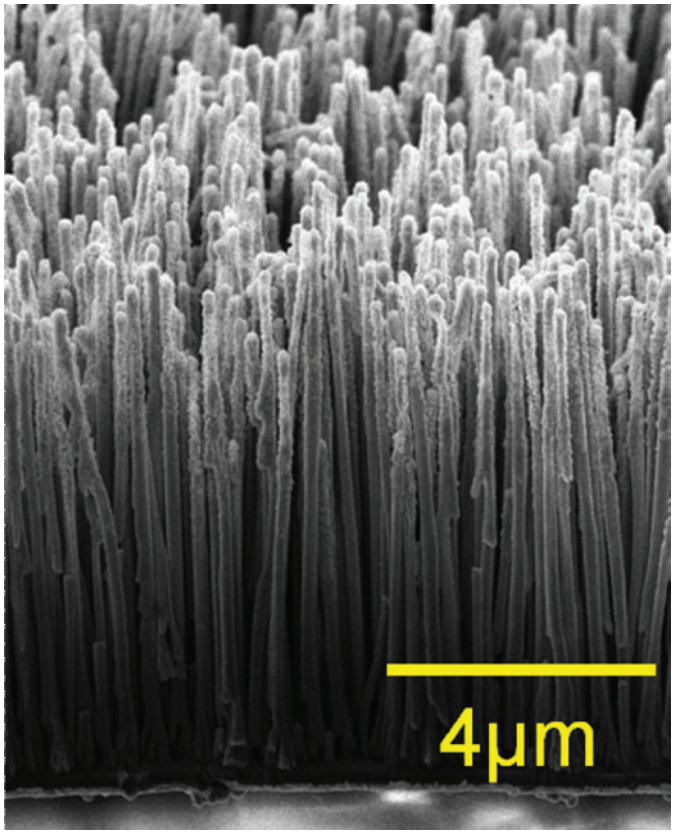


Figure 5. SEM image of 8 μm tall vertically aligned copper nanowires attached to a silicon substrate.

2.3 Packaging

As shown in Figure 6, the test chip is packaged on a printed circuit board (PCB) by a flip-chip bonding process. The gap between the chip and PCB was filled with underfill material, FP4549 (Henkel), to reduce any unwanted boiling at the edge of and underneath the chip.

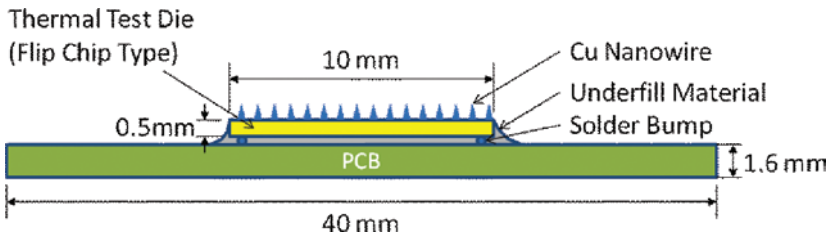


Figure 6. Test chip package.

2.4 Test setup

The schematic of the experimental setup is shown in Figure 7. The tests were conducted inside a transparent jacketed glass beaker with dielectric coolant PF-5060 as the working fluid. A condenser coil to condense the vapor was located in the top portion of the jacketed beaker, and the cooling rate and temperature of the condensing coil were controlled by a power supply according to the local operating conditions. Additionally, a T-type thermocouple was inserted into the jacketed beaker to measure the temperature of the working fluid. Power to the thermal test chip was supplied by an Agilent E3645A power supply, and the measured resistance was converted to temperature using the formulated calibration curve (details of chip calibration are provided in the next section). A NI LabVIEW program was used to control the power supply and the data acquisition system. The measurement data obtained was stored once steady state conditions were reached for each power input.

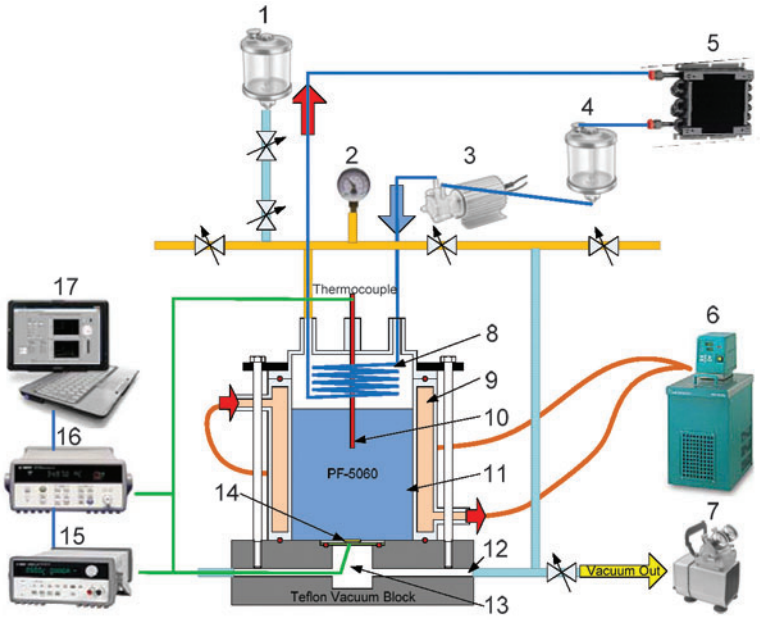
The premier importance for any boiling experimental setup is to minimize the heat loss to the surroundings. Several key designs choices were made for this purpose. First, the jacketed beaker was designed so that water could be used to maintain a constant sidewall temperature. The jacketed beaker has an inner chamber that contains the PF-5060, and an outer chamber with a closed flow path around the perimeter of the inner chamber. The jacketed beaker has inlet and outlet ports that were connected to a heat exchanger, and the heat exchange setpoint was adjusted so that the sidewall temperature were maintained at 56˚C. Secondly, the jacketed beaker was mechanically attached to a Teflon block using a clamp and an o-ring. The Teflon block has a square recess that is used to hold the packaged thermal test chip in place. Beneath the thermal test chip is a deeper recess that has two ports. One port is used for electrically wiring and thermocouples. The other port is used to pull a vacuum on the backside of the packaged thermal test chip. Creating a vacuum condition on the backside of the thermal test chip limits heat loss to the surroundings. Finally, the bottom of the Teflon block is placed on a heater and heated so that a non-powered thermal test chip reads 56˚C. In summary, a heat exchanger with water is used to prevent heat loss of the working fluid through the side walls of the boiling chamber. In addition, a heated Teflon block, with a vacuum condition on the backside of the thermal test chip, is used to prevent heat loss through the bottom of the boiling chamber. [19].

2.5 Test procedure

2.5.1 Test chip calibration

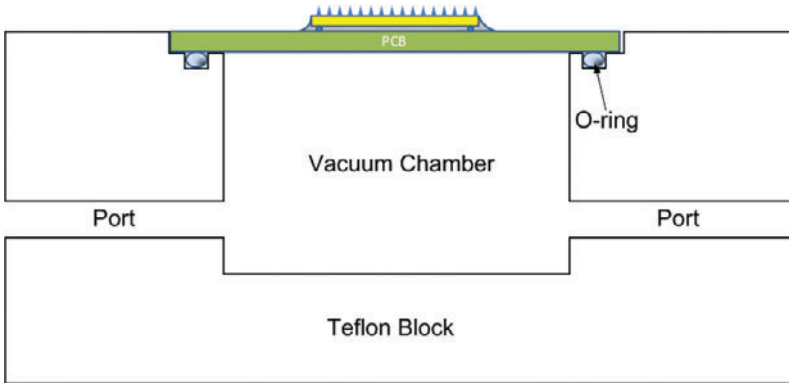
The platinum resistor provides simultaneous power delivery and temperature sensing capabilities. Since the resistance of the heater is a function of temperature, the thermal test chip surface temperature can be measured from resistance variation. To determine this relationship, a T-type thermocouple is placed near the thermal test chip. Both the thermal test chip and the thermocouple are placed in an oven. The oven is set to different values of temperature ensuring that the entire operating range of the

experiments is covered. The resistance, obtained from the supplied voltage and the corresponding current, is plotted against the thermocouple temperature measurements. A linear curve is fit through the data, and that function is used to determine the thermal test chip surface temperature from the calculated resistance.



1. Reservoir
2. Pressure Gage
3. Water Pump
4. Reservoir
5. Heat Exchanger
6. Heat Exchanger
7. Vacuum Pump
8. Condenser
9. Outer Chamber
10. Thermocouple
11. Inner Chamber for Working Fluid
12. Ports
13. Vacuum Chamber
14. Test Device
15. DC Power Supply
16. Data Acquisition system
17. Computer

(a)



(b)

Figure 7. Schematic of the pool boiling test apparatus: Overview; (b) Teflon Block.

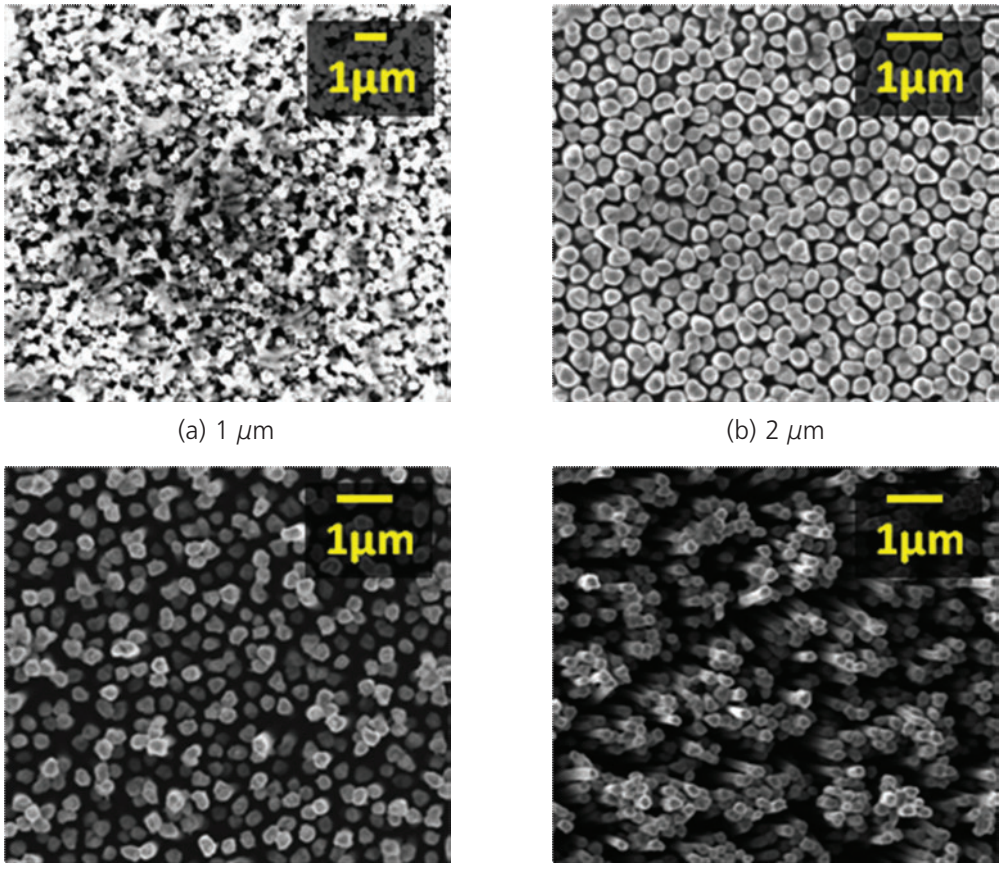
2.5.2 Measurement

Experiments were conducted at saturation condition at room pressure. Prior to this, the fluid was degassed by boiling it vigorously for an hour. After degassing, the experiment was run by supplying power to the test surface. All the measurements were monitored using LabVIEW, and at each power input, data were recorded once the embedded RTD reached steady state condition. Since the RTD is located on the opposite side of the thermal test chip in comparison to the location of the copper nanowires, the actual surface temperature was inferred from the RTD measurement. The temperature difference between the surface temperature and the RTD was calculated by assuming one-dimensional heat transfer through the silicon substrate, and by multiplying the power input to the RTD by the estimated thermal resistance between the RTD and surface. An average of at least ten measurements was taken at each steady state for improved accuracy.

3. RESULTS AND DISCUSSION

3.1 Effect of nanowire length

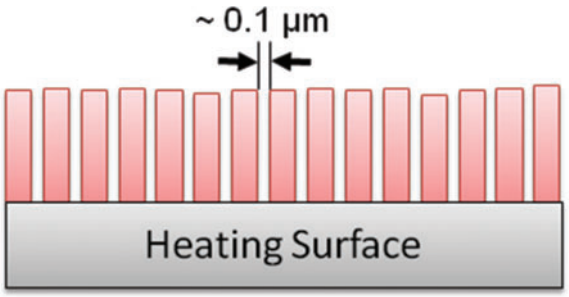
The length of copper nanowires was the parameter of interest in this study. Figure 8 shows scanning electron microscope (SEM) images of copper nanowires having different lengths (1 μm, 2 μm, 4 μm, and 8 μm). However, as a result of the fabrication process, a covariate, cavity size, appeared as a dependent parameter. For the nanowire lengths considered, there are three different cavity sizes: nanowire spacing, surface cavities, and deep cavities. Representations of these cavities are shown in Figure 9.



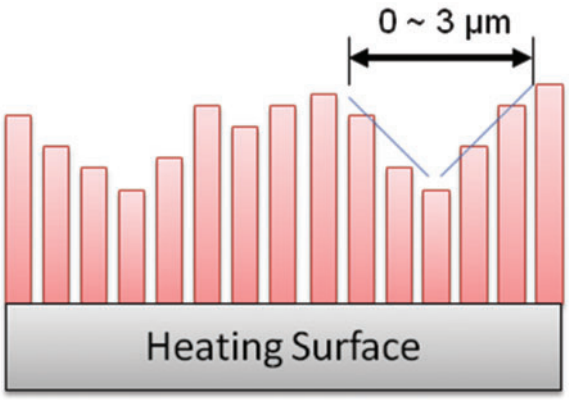
(a) 1 μm (b) 2 μm

(c) 4 μm (d) 8 μm

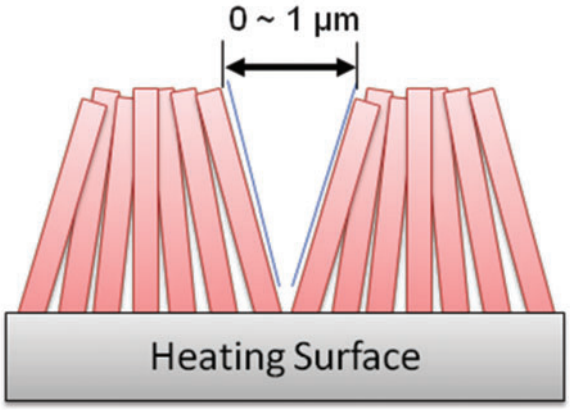
Figure 8. Top down SEM image of copper nanowires having different length (1 μm, 2 μm, 4 μm, 8 μm).



(a)



(b)



(c)

Figure 9. Three different cavity sizes: (a) nanowire spacing; (b) surface cavities; (c) deep cavities.

The first cavity, nanowire spacing, is present for all the samples and is defined by the AAO template pore pitch and size. This cavity is the gap between adjacent vertically aligned nanowires, and for the samples of interest, the gap is on the order of several tens of nanometers in magnitude. In addition to the natural template spacing between nanowires, there are surfaces cavities. These cavities result from the electroplating process. After electroplating, there is a variation in nanowire length. As the average nanowire length increases, the variation also increases. This leads to random, but frequent, divots at the free end of the nanowires, as shown in Figure 10. The resulting surface cavities range from 0.3 μm to 3 μm for the 1 μm to 8 μm samples respectively.

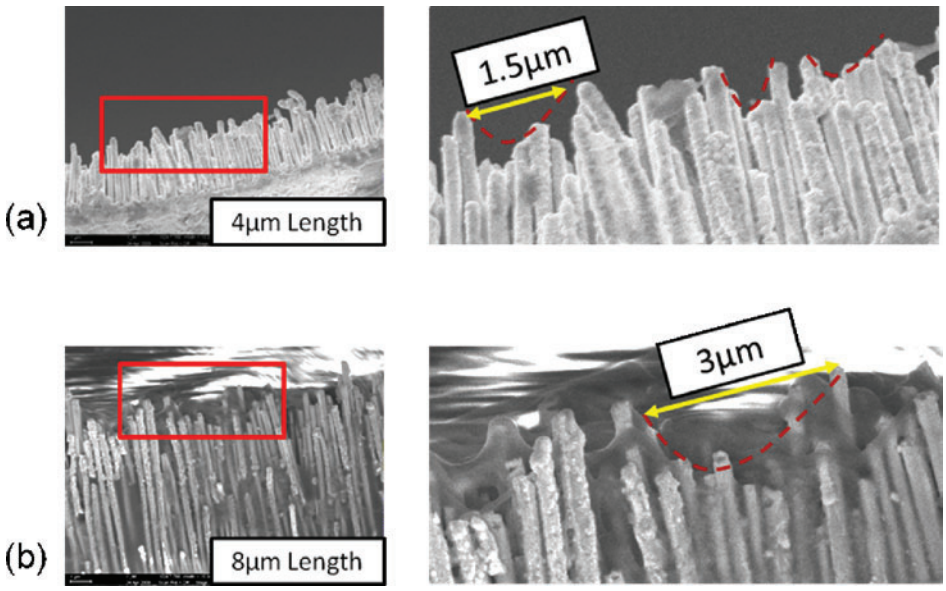


Figure 10. SEM image showing longer nanowires have bigger cavities: (a) 4 μm wire length; (b) 8 μm wire length.

Finally, the last cavity formation is also attributed to the fabrication process. After the AAO template is dissolved and the copper nanowires are released, the sample is allowed to dry. The evaporation process causes the structures to pull together as a result of the water surface tension. Longer nanowires will tend to form larger groups due to the larger surface tension force. As seen in Figure 8, the coalescence cavity size varies from no cavity to 1 μm, as the sample length increases from 1 μm to 8 μm. Although the primary factor of interest in this study is the length of the copper nanowires, the fabrication process lead to the formation of cavities which also affect the boiling performance.

Before testing the nanowire samples, the CHF for smooth silicon devices, the baseline testing condition, were measured and compared to prior literature. For the current system, three baseline samples were tested under saturation conditions at room pressure and one of the results is shown graphed with the results of prior literature, as shown in Figure 11.

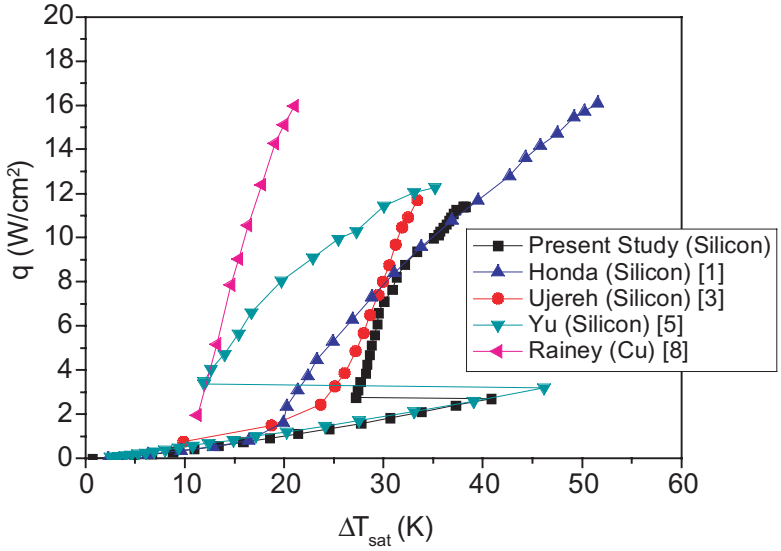


Figure 11. Comparison of boiling curves for baseline test.

The CHF for the present measurements ranged from 11 to 13 W/cm^2, and slope and location of curve compared well with previous published results. The relatively large variation between boiling curves in Figure 11 can be attributed to heat loss, non-uniform heating, temperature measurement location/method, sample edge treatment, and surface contamination for different experiments. This result shows that the experimental setup provides accurate measurements within the variation of previous publications.

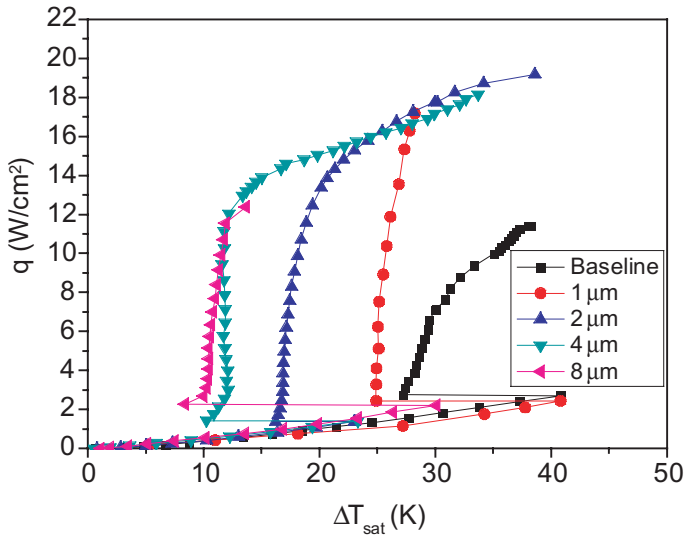


Figure 12. Effect of nanowire length.

Following the baseline testing, boiling curves for the nanowire samples of interest are shown in Figure 12. There are three trends that need to be discussed: CHF, incipience temperature, and wall superheat in the nucleate boiling regime. First, there appears to be an optimum CHF value with regards to the length of the copper nanowire arrays. Figure 13 highlights this optimum point by plotting the CHF value as a function of wire length. As one can see in Figure 13, the CHF value increases from 11.4 W/cm^2 for the baseline sample, to a maximum of 19.2 W/cm^2 for the sample with nanowires of 2 μm length. The CHF value then decreased to 12.4 W/cm^2 as the sample length increases up to 8 μm.

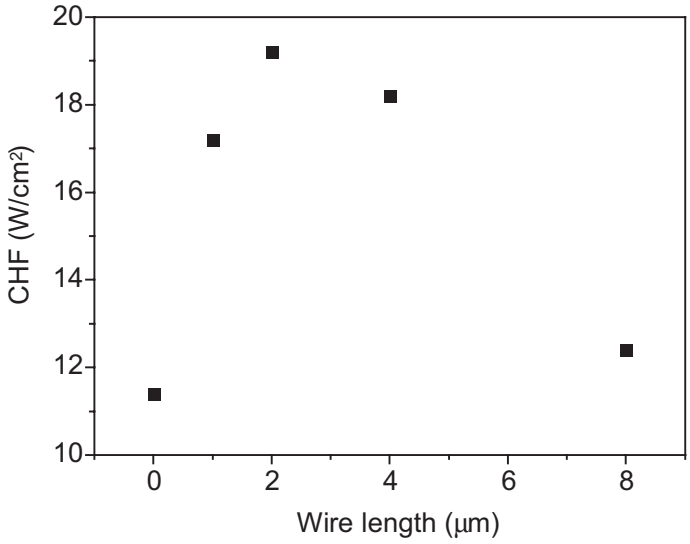


Figure 13. Effect of nanowire length on CHF values.

The reason for an optimum CHF value is the interplay between wettability and vapor detachment. As the structures increase in length, the capillary force that pulls the liquid to the surface increases. However, at the same time, the liquid flow resistance also increases. This leads to an optimum length for the copper nanowires. Structures shorter than the optimum will not be benefiting enough from the improved wetting that a nanostructured surface offers. However, if the structures are too long, the surface enhancement becomes detrimental, because the fluid is unable to effectively wet the interface. The interplay is further compounded by the vapor detachment process. Longer structures restrict the movement of vapor by causing a larger drag force, and as a result, tend to trap the vapor between the wires. Trapped vapor results in lower CHF values, since dryout is easier to achieve. These factors create a complicated exchange that ultimately yields an optimum length of 2 μm. The optimal length of the nanowires is expected to vary with the working fluid and nanostructure geometry, such as the diameter, pitch, and magnitude of coalesence.

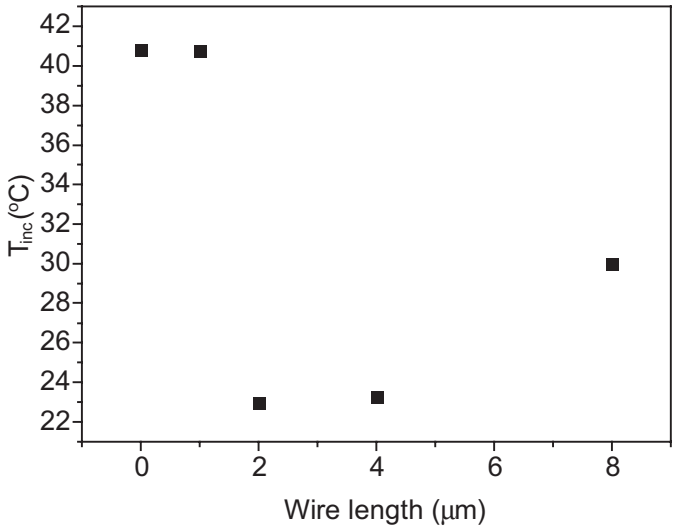


Figure 14. Effect of nanowire length on incipience temperature.

In addition to the CHF trend, the incipience temperature was found to also have an optium value at a copper nanowire length of 2 μm. For the 4, 6, and 8 μm tall samples, this could be due to the increase in vapor flow resistance as the wire length increases. Since the bubbles are generated at the silicon-nanowire interface, vapor bubbles have to travel further to reach the bulk liquid as the nanowire length increases. It was also observed that, the CHF was higher when the incipience temperature was lower for these samples. This supports the hypothesis that CHF and incipience temperature are affected by the flow resistance of the trapped vapor bubbles. On the other hand, for the 1 μm tall sample, the lack of micro-sized surface cavities, as depicted in Figure 9b, increases the incipence temperature. Essentially, the 1 μm tall sample lacks micro-sized nucleation sites which is necessary for boiling at lower superheat.

The final trend seen in Figure 12 is the variation in surface superheat within the nucleate boiling regime. From the experimental results, it can be inferred that the wall superheat in the nucleate boiling regime decreases, as the nanowire height increases. This result is in agreement with Hsu's model [20] that states, for the cavities sizes considered in the present study, the surface superheat in the nucleate boiling regime increases as the cavitiy size decreases. The 8 μm tall sample benefits from the 1 μm sized cavity from coalesence effects, the 3 μm sized cavity from the variation in structure height, and the 100 nm spacing between the nanowires. However, the 1 μm tall nanowire sample only has the 100 nm spacing as a potential nucleation site.

3.2 Repeatibility and Hysteresis Study

Repeated experiments were performed with the copper nanowire samples to observe the possibility of hysteresis. From Figure 15, which displays the repeated experimental runs for a 2 μm sample, it can be observed that the incipience temperature for boiling for the first run was higher than the subsequent runs. This could be because the vapor trapped between the nanowires at the conclusion of an experiment would lower the amount of superheat required to initiate boiling for the next set of runs. When the power supply was cut off after the CHF was achieved, small bubbles were observed emanating from the surface. When the bubble size decreases, surface tension forces dominate the buoyancy forces, and hence, the bubble remains attached to the surface. The plot of incipience temperature for 4 μm copper nanowires boiling for different runs is shown in Figure 16. It can be seen from the figure that boiling incipience temperature decreased for subsequent runs, and increased again after a 24 hour break in experimental runs.

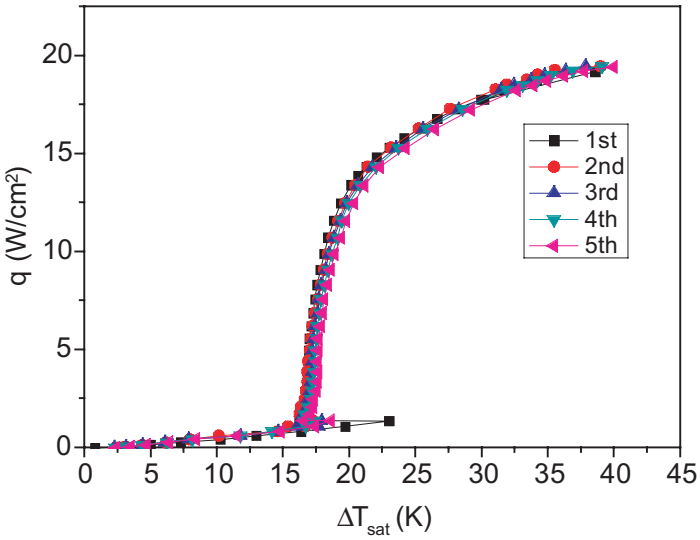


Figure 15. Comparison of boiling curves of repeat test for 2 μm.

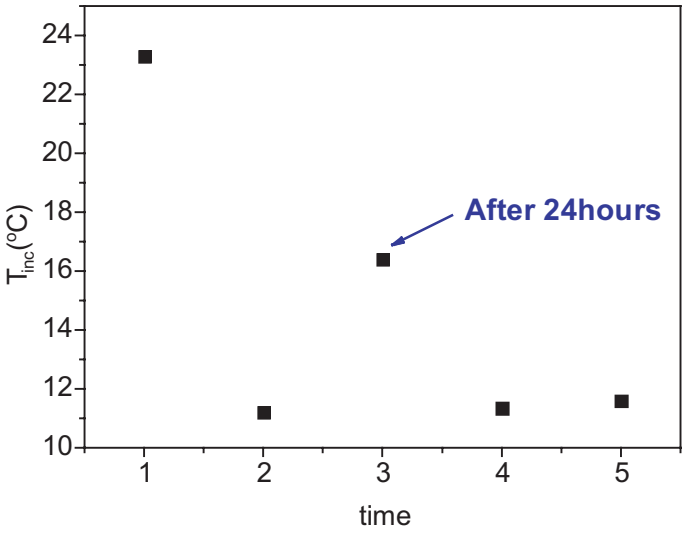


Figure 16. Incipience temperatre versus time for 4 μm sample. The incipience temperature increased after a 24 lull in experiemental runs.

After performing the experiments with nanowires of different lengths, the variation in the boiling curves is the smallest with 2 μm long copper nanowires. This is most likely a result of the number of vapor bubbles trapped in between the shorter nanowires is fewer.

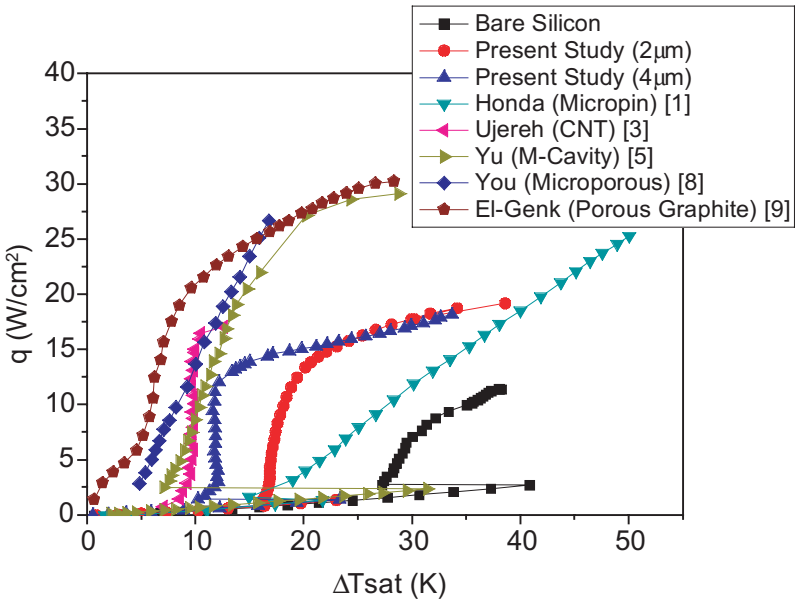


Figure 17. Present study's results compared to previously published surface modifications with the same working fluid.

Figure 17 compares the boiling curve with ΔT_{sub} =0 K for several enhancement techniques for PF-5060 or FC-72. FC-72 has the same boiling point and similar thermal and fluidic properties to PF-5060 which is why the results are included. The maximum CHF (30.3 W/cm^2) was achieved using porous graphite [13]. The maximum CHF found in this study was 19.5 W/cm^2, with 2 μm tall copper nanowires. As mentioned before, the unique feature of the present study is nucleate boiling enhancement for sub 100 μm spaces. Figure 18 summarizes the performance of the samples studied as a function of cooling rate versus surface modification size. On a per μm scale, the copper nanowire arrays offer a considerable heat transfer improvement on the order of a factor of ten larger than other enhanced features. By further optimizing the dimensions and structure of nanowires, improved performance is anticipated.

4. CONCLUSIONS

To fabricate a high performance boiling surface, copper nanowire arrays on a Si substrate are fabricated by electro-chemical deposition through an AAO template. It is observed that copper nanowires increase the critical heat flux and reduce the wall superheat compared to the baseline experiments performed using a smooth silicon surface. The copper nanowires increase the critical heat flux by improving the surface wetting as a result of the generated capillary force. In addition, nanowires increase the number of boiling nucleation sites, which leads to a higher heat transfer coefficient. In the experiments, the performance of copper nanowires is found to depend on the wire height. Incipience temperature for boiling was found to increase as the nanowire height increases, an optimum value of CHF was found at 2 μm, and the superheat for nucleate boiling regime decreases as the nanowire height increases.

Copper nanowires are highly conductive, are effective at short lengths, and can be integrated with future semiconductor cooling methodologies. Nanowires can be used to further increase the heat transfer in microchannels with sizes of 100 μm or less without greatly affecting the pressure drop. The

work reported here is an enhancement over previous studies on structured surfaces, which mainly considered structures on the order of 100 μm.

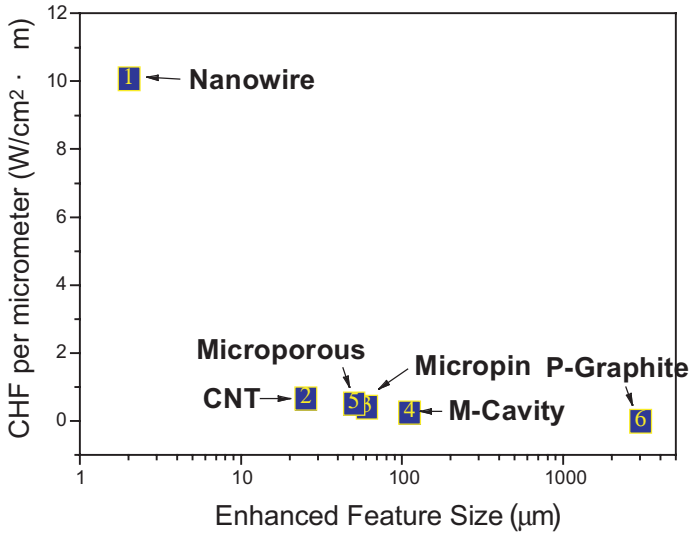


Figure 18. CHF vs. surface enchancement length for the cu nanowires used in this study and other surface modifications in the literature.

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