Gate Current Modeling and Optimization of High-k Gate Stack MOSFET Structure in Nano Scale Regime

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ABSTRACT
In this paper, an analytical model has been developed for gate tunneling current in nano scale MOSFET with high-k dielectric stack as gate insulator. A computationally efficient model for gate tunneling current through different high-k gate stack structure is presented. The proposed model has been successfully used for different gate stack dielectric simply by adjusting two fitting parameters. The model predictions are compared with the two-dimensional Santaurus device simulation. Good agreement between the model predictions and device simulation results has been obtained. The effects of interfacial oxide thickness, type of gate stack and reverse gate stack on the gate tunneling current have also been studied as a function of gate voltages for a given equivalent oxide thickness (EOT) of 1.0 nm. It was also shown that smaller inter oxide layer thickness reduces gate leakages current with the introduction of high-k gate stack structure in place of individual high-k dielectric or SiO_2.

Keywords: MOSFET, inelastic trap assisted tunnelling, gate tunneling current, high-k stack, DIBL, SS

1. INTRODUCTION

Since the early 1970s, we have witnessed a relentless drive toward smaller features of complementary metal-oxide-semiconductor (CMOS) transistors and hence higher functionality on semiconductor chips. To meet the requirement of high performance, scaling of MOSFETs toward shorter channel lengths requires thinner gate oxides and higher doping levels in order to achieve high drive currents and minimized short-channel effects [1–2].

Currently, for MOSFET applications, traditional SiO_2 gate oxide is quickly approaching its physical scaling limit due to severe gate tunneling leakage [3]. To reconcile the need for reduced gate leakage current in highly scaled devices, the replacement of SiO_2 as gate dielectric with alternate high-k dielectric material is considered as a method to contain/reduce the gate leakage current [4–8].

Research on high-k dielectrics quickly converged on the Al_2O_3, HfO_2, and ZrO_2 family, which has a band gap larger than 5.0 eV [9–13]. However, HfO_2 and ZrO_2 received most attention based on their better thermal stability with Si [14, 15]. The main concern for high-κ dielectrics include several orders of magnitude more traps found in the bulk or interface [14–17].Consequently, trap-assisted gate tunneling current cannot be neglected in comparison with direct tunneling current and must be taken into account when calculating/modeling the gate current for nanoscale CMOS devices in modern simulators. The fact is also supported by [18] according to which it is necessary to take into account

the inelastic tunneling assisted by traps for gate insulator physically thicker than 2.6 nm which is the case for high-k gate insulator.

Experiments have shown that the direct substitution of high-k gate dielectric without an interfacial oxide leads to the degradation of field effect transistor FET drive current by ~2 in n-channel devices, and > 50 in p-channel devices [19, 20]. A unified model suitable for investigation of multiple dielectric high-k stack structures is therefore in need.

In the past, modeling of the gate tunneling currents through high-k stack structures of nano Scale MOSFETs has been treated numerically in [21–25]. In a recent paper [26], W.B. Chen et al developed a simplified analytic model on tunneling current of sub-micron MOSFET based on the models in Ref. [27] but neglected the trap assisted tunneling through high-k stack structure.

In this work, a computational efficient analytical model of gate tunnel current through high-k stack structure is presented which accounts for trap assisted tunneling mechanism. This model is based on an inelastic trap-assisted tunneling mechanism combined with semi-empirical gate leakage current model of BSIM 4. This model calculates the gate tunneling current with energy loss (E_{loss}) during inelastic trap assisted tunneling process and $\alpha_{(ch/ov)}$ as fitting parameters. It is conceptually simple, computationally efficient and gives very consistent results with Synopsys Santaurus Simulator.

The rest of the paper is organized as follows. In Section II, theoretical modeling of trap assisted gate tunneling current is established. The high-k gate stack device structure and design used for simulation set up is presented in Section III. The results obtained are discussed in Section IV. Finally, concluding remarks are offered in Section V.

2. THEORETICAL GATE CURRENT MODEL

The schematic energy band diagram shown in Fig. 1 illustrate our model in more detail showing the conditions which lead to inelastic trap assisted tunneling. One path is to tunnel directly through the top of energy band into the probe tip (J_{in}), and the other path is to tunnel via the isolated traps within the gate insulator (J_{out}).

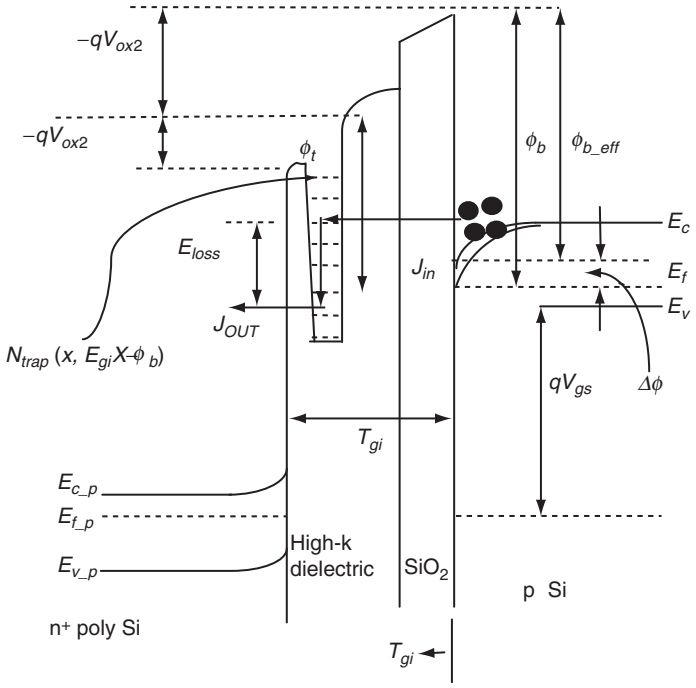

Figure 1. Energy band diagram showing the two step inelastic trap assisted tunneling through stacked high-k gate dielectrics.

Assumptions:

i) inelastic trap assisted tunneling is a two step process for simplicity.
ii) Firstly, electrons tunnel into deep lying trap state, become released from the trap state and subsequently tunnel to gate under the influence of the applied electric field.
iii) the Si substrate and the poly Si form a parallel plate capacitor with two dissimilar dielectrics i.e. pure SiO_2 and high-k and is known as composite gate dielectric (High-k and pure SiO_2).

In the modeling process, tunneling-in current from inversion layer to the traps and tunneling-out current from the traps to the gate are calculated by modifying the formulation of direct tunneling in the BSIM 4 model [28–29]. Assuming that x is the distance from the Si–SiO_2 interface, $N_{trap}(x, E)$ is the sheet trap density in cm^2 at a distance x and having the energy level with respect to the conduction band edge of gate dielectric, $O_t(x, E)$ is the electron occupancy of the traps at a distance of x and the energy of E, σ_t is the capture cross section of the traps and A_g is the gate tunneling area. The tunnel-in current density (J_{in}) into the traps and the tunnel-out current density (J_{out}) from the traps are then expressed as

$$J_{in} = \frac{q}{A_g}\sigma_t N_{trap}\left(x,\, qE_{gi}x - \phi_{b\_eff}\right).\times\left[1 - O_t\left(x,\, qE_{gi1}x - \phi_{b\_eff}\right)\right]J_1\left(\phi_{b\_eff},\, x,\, E_{gi1}\right) \tag{1}$$

$$J_{out} = \frac{q}{A_g}\sigma_t N_{trap}\left(x, qE_{gi1}x - \phi_{b\_eff}\right).\times O_t\left(x, qE_{gi1}x - \phi_{b\_eff}\right)J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right) \tag{2}$$

$$\phi_t = \phi_{b\_eff} - qE_{gi1}x + E_{LOSS} \tag{3}$$

where Φ_t is the barrier height of the gate insulator trap states, E_{gi} is the electric field in the gate insulator, E_{gi1} is the electric field over a distance x of the trap relative to the interface in the gate insulator and E_{gi2} is the electric field over a distance t_{gi}-x relative to the interface in the gate insulator, E_{Loss} is the energy loss accompanied with the injection of electrons into the neutral trap sites and σ_t is assumed to be constant irrespective of the position and energy level of the traps. J_1 and J_2 are the uniform current densities and are calculated by modifying the formulation of direct tunneling in the BSIM 4 model. ϕ_b is the interface barrier height. It is taken as the average of interface barrier height of oxide and high-k gate layer individually. So

$$\phi_b = \frac{\left(\phi_{b\_ox} + \phi_{b\_hk}\right)}{2} \tag{4}$$

where ϕ_{b_hk} is the barrier height of high-k gate layer, ϕ_{b_ox} is the barrier height of oxide layer and ϕ_{b_eff} is the effective barrier height, given as below,

$$\phi_{b\_eff} = \phi_b - \Delta\phi \tag{5}$$

$$\Delta\phi = \sqrt{\frac{qE_{gi}}{4\pi\varepsilon_{eff}}} = \sqrt{\frac{qV_{gi}}{4\pi\varepsilon_{eff}T_{gi}}} = \left(\frac{2q^3 N_{DTC(ch)}\phi_{b\_eff}}{16\pi^2\varepsilon_{eff}^3}\right)^{1/4} \tag{6}$$

The $\Delta\phi$ is the reduction in the barrier height at the high-k/SiO_2/Si interface [30] from Φ_b so that barrier height becomes ϕ_{b_eff}. This reduction in barrier height is due to image charges across the interface. This barrier reduction is of great interest since it modulates the gate tunneling current. $N_{DTC(ch)}$ is the effective density of carrier in channel and ε_{eff} is the equivalent dielectric constant of composite gate dielectric. We have found the equivalent dielectric constant of the composite gate dielectric in terms of the oxide thickness by considering the MOSFET as parallel plate capacitor with two dissimilar dielectrics.

$$\varepsilon_{eff} = \left[\frac{t_{ox}}{\varepsilon_{ox} t_{gi}} + \frac{t_{gi} - t_{ox}}{\varepsilon_{hk} t_{gi}} \right]^{-1} \tag{7}$$

where ε_{eff}, ε_{ox} and ε_{hk} are the dielectric constants of the equivalent dielectric, the pure SiO_2, and the high-k gate dielectric respectively, t_{gi} is the total thickness of the gate dielectric, and t_{ox} is the thickness of the pure silicon dioxide layer.

The resulting tunneling current J_{ITAT} of this trap-assisted tunneling process is given by a detailed balance of J_{in} and J_{out}. Consequently, inelastic trap assisted tunneling current can be expressed as

$$J_{ITAT} = \frac{q}{A_g} \sigma_t N_{trap} \left(x, qE_{gi}x - \phi_{b\_eff} \right) . P_{ITAT} \left(x, E, E_{gi} \right) \tag{8}$$

where P_{ITAT} can be expressed as

$$P_{ITAT} = \frac{J_1 \left(\phi_{b\_eff}, x, E_{gi1} \right) . J_2 \left(\phi_t, t_{gi} - x, E_{gi2} \right)}{J_1 \left(\phi_{b\_eff}, x, E_{gi1} \right) + J_2 \left(\phi_t, t_{gi} - x, E_{gi2} \right)} \tag{9}$$

Using Gauss's law and considering MOS capacitor equivalent circuit, the local electrical fields E_{gi1} and E_{gi2} of both the tunneling regions finally become

$$E_{gi1} = E_{gi} + \frac{t_{gi} - x}{t_{gi}} . \frac{qN_{trap}}{\varepsilon_{eff}} \tag{10}$$

$$E_{gi2} = E_{gi} + \frac{x}{t_{gi}} . \frac{qN_{trap}}{\varepsilon_{eff}} \tag{11}$$

The modified uniform current density J_1 and J_2 as obtained from BSIM 4 are expressed as

$$J_1 \left(\phi_{b\_eff}, x, E_{gi1} \right) = A_t \frac{C \left(\phi_{b\_eff}, x, E_{gi1} \right)}{\phi_{b\_eff}} . \times \exp \left[- \frac{8\pi \sqrt{2m_{eff}}}{3hq} . \frac{\phi_{b\_eff}^{3/2}}{E_{gi1}} \beta \left(\phi_{b\_eff}, x, E_{gi1} \right) \right] \tag{12}$$

$$J_2 \left(\phi_{b\_eff}, x, E_{gi1} \right) = A_t \frac{C \left(\phi_t, t_{gi} - x, E_{gi2} \right)}{\phi_t} \times \exp \left[- \frac{8\pi \sqrt{2m_{eff}}}{3hq} . \frac{\phi_t^{3/2}}{E_{gi2}} \beta \left(\phi_t, t_{gi} - x, E_{gi2} \right) \right] \tag{13}$$

where $A_t = \dfrac{q^3}{8\pi \phi_{b\_eff} \varepsilon_{eff}}$

$$c_{(ch,ov)} \left(\phi_{b\_eff}, x, E_{gi1} \right) =$$

$$\exp \left[\frac{20}{\phi_{b\_eff}} \left(\frac{x \left| E_{gi1(ch,ov)} \right| - \phi_{b\_eff}}{\phi_{b\_eff}} + 1 \right)^{\alpha(ch,ov)} . \left(1 - \frac{x \left| E_{gi1(ch,ov)} \right|}{\phi_{b\_eff}} \right) \right] . \times \left(E_{gi1} \right) . N_{DTC(ch,ov)}$$

$$c_{(ch,ov)}\left(\phi_t, t_{gi}-x, E_{gi2}\right)=$$
$$\exp\left[\frac{20}{\phi_t}\left(\frac{(t_{gi}-x)\left|E_{gi2(ch,ov)}\right|-\phi_t}{\phi_t}+1\right)^{\alpha(ch,ov)}.\left(1-\frac{(t_{gi}-x)\left|E_{gi2(ch,ov)}\right|}{\phi_t}\right)\right]\times.\left(E_{gi2}\right).N_{DTC(ch,ov)}$$

$$\beta(\phi_{b\_eff}, x, E_{gi1})=1-\left(1-\frac{qx}{\phi_{b\_eff}}\left|E_{gi1}\right|\right)^{3/2}$$

$$\beta(\phi_t, t_{gi}-x, E_{gi2})=1-\left(1-\frac{q\left(t_{gi}-x\right)}{\phi_t}\left|E_{gi2}\right|\right)^{3/2}$$

$$N_{DTC(ch)}=\begin{cases}\dfrac{\varepsilon_{eff}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1+\exp\left(-\dfrac{\left(V_g-V_{FB}\right)}{n_{acc}v_t}\right)\right]\right. for\ V_g<0\\ \dfrac{\varepsilon_{eff}}{t_{gi}}\left\{n_{inv}v_t.\ln\left[1+\exp\left(-\dfrac{\left(V_g-V_{th}\right)}{n_{inv}v_t}\right)\right]\right. for\ V_g>0\end{cases}$$

$$N_{DTC(ov)}=\begin{cases}\dfrac{\varepsilon_{eff}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1+\exp\left(-\dfrac{V_g}{n_{acc}v_t}\right)\right]\right. for\ V_g<0\\ \dfrac{\varepsilon_{eff}}{t_{gi}}\left\{n_{acc}v_t.\ln\left[1+\exp\left(-\dfrac{V_{ge}}{n_{acc}v_t}\right)\right]\right. for\ V_g>0\end{cases}$$

and m_{eff} is the equivalent effective mass of the composite dielectric with pure SiO_2 and high-k gate dielectric. Taking the resistances in series of the two layers of the gate dielectric, we have

$$R_{gi}=R_{ox}+R_{hk} \tag{14}$$

Considering the relaxation time $\tau_{ox}=\tau_{hk}=\tau_{eff}=\tau$, we obtain the equivalent effective mass using Eq. (14) as

$$m_{eff}=\left[\frac{m_{ox}t_{ox}}{t_{gi}}+\frac{m_{hk}\left(t_{gi}-t_{ox}\right)}{t_{gi}}\right] \tag{15}$$

In the above equation, $\alpha_{(ch,ov)}$ is the fitting parameter depending upon channel or source/drain overlap tunneling, ϕ_b is the actual tunneling barrier height, n_{inv} and n_{acc} are the swing parameters, V_{FB} represents the flat band voltage, $N_{DTC(ch,ov)}$ denotes the density of carrier in channel/overlap region depending upon MOSFET biasing condition and V_{ge} is the effective gate voltage excluding poly gate non-uniformity and gate length effect and is equal to $V_{ge} - V_{poly}$. The default values of n_{inv} and n_{acc} are S/v_t (S is the sub threshold swing) and 1 respectively. The correction factor ($C_{F(ch,ov)}$) and transmission probability

($T_{WKB(ch,ov)}$) are different for channel and source/drain overlap region because both channel and overlap component have different value of $V_{ox(ch,ov)}$ and $N_{DTC(ch,ov)}$. It is because of the fact that overlap region has almost zero flat band voltage as both Source Drain Extension (SDE) region and overlying poly-gate Si are heavily doped n^+ regions. The $N_{DTC(ch,ov)}$ has been given differently for both region as above. m_{ox} is the effective mass of electrons in the SiO_2 layer and m_{hk} is the same in the high-k gate dielectric layer. The voltage across the gate insulator for different region of operation is as follows.

$$V_{gi} = \begin{cases} \left(V_g - \phi_s - V_{FB}\right) \; for \; V_g < 0 \\ \left(V_{ge} - \phi_s - V_{FB}\right) for \; V_g > 0 \end{cases} \tag{16}$$

Where ϕ_s is the surface band bending of the substrate and are calculated for channel and overlap region depending upon the biasing condition of the MOSFET device including the poly non-uniformity, gate length effects and image force barrier lowering. The accurate surface potentials expressions in case of channel in weak inversion/depletion, strong inversion and in accumulation can be taken from [31]. The gate effective voltage including the effect of nonuniform dopant distribution in the gate is derived as follows.

$$\therefore V_{ge} = (V_{FB} + \phi_{so} - \Delta V_{p1} - \Delta V_{p2}) + \frac{\left(q\varepsilon_{si} N_{poly} T_{gi}^2\right)}{\varepsilon_{ox}^2}\left[\sqrt{1 + \frac{2\varepsilon_{ox}^2 (V_g - V_{FB} - \phi_{so})}{q\varepsilon_{si} N_{poly} T_{gi}^2}} - 1\right] \tag{17}$$

The ϕ_{so}, by taking the quantization effect into account, is given [32] as follows

$$\phi_{so} = 2\phi_s + \Delta\phi_s^{QM} - V_{BS} \tag{18}$$

where $\Delta\phi_s^{QM}$ can be taken from [31]. Equation (17) includes the non uniformity in the gate dopant profile through a term ΔV_{p1} and fringing field effect *i.e* gate length effect through a term ΔV_{p2}. The potential drop ΔV_{p1} due to non uniform dopant profile in poly Si gate, caused by low energy ion implantation, is given [33] by

$$\Delta V_{p1} = \left(\frac{kT}{q}\right) \ln\left(\frac{N_{poly\_top}}{N_{poly\_bottom}}\right) \tag{19}$$

The N_{poly_top} and $N_{pol\bar{y}\_bottom}$ are the doping concentration at the top and bottom of the polysilicon gate. The potential drop ΔV_{p2} due to gate length effect, caused by very short gate lengths is given as below

$$\Delta V_{p2} \approx \frac{\Delta Q}{C_d} = \frac{2qAN_d}{L_g C_d}\left(V/cm\right) \tag{20}$$

$$C_d = \delta \frac{\varepsilon_{eff}}{\pi} \ln\left[\frac{3 - \cos\left\{\pi\left(\frac{T_F - T_{gi}}{T_F}\right)\right\}}{1 + \left\{\pi\left(\frac{T_F - T_{gi}}{T_F}\right)\right\}}\right] \tag{21}$$

where A denote the triangular area of the additional charge, L_g is the gate length, C_d is the depletion capacitance in the sidewalls [34], ε_{eff} is the effective permittivity of the composite gate insulator, T_F is the thickness of the field oxide, T_{gi} is the thickness of the gate insulator and δ is fitting parameter equal to 0.95 normally.

3. SIMULATION SET UP

Figure 2. shows the schematic of device structure of N-MOSFET with high-k gate stack dielectric used in this study.

The deep S/D region is composed of a heavily doped silicon and a silicide contact. The doping of the silicon S/D region is assumed to be very high, 1×10^{20} cm^{-3}, which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 50 nm long and 20 nm high. This gives a large contact area resulting in a small contact resistance. The doping concentration of the acceptors in silicon channel region is assumed to be graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of 1×10^{18} cm^{-3} and 1×10^{17} cm^{-3} near the channel. The halo implantation done around the S/D also reduces short-channel effects, such as the punch-through current, DIBL, and threshold voltage roll-off.

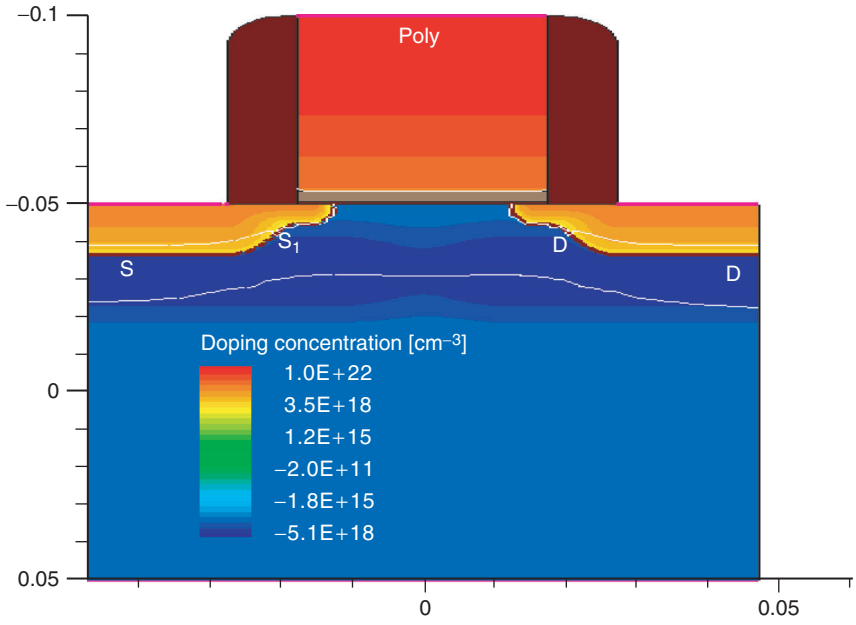

Figure 2. NMOSFET device structure with stacked high-k gate dielectrics used in simulation.

The MOSFET has a 50-nm-thick n^+ poly-Si gate with metallurgical gate length of 25 nm and a 1.0 nm gate oxide. The doping concentration in polysilicon gate is 1×10^{22} cm^{-3} at the top and 1×10^{20}cm^{-3} at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and poly silicon. The oxide spacer has been assumed to reduce the gate capacitance. Here, Lo represents the overlap length, which is controlled by the S/D implantation energy. Lo = 5 nm optimized with off current is used in this work. The MOSFET with L_{met} of 25 nm was designed to have a V_T of 0.19 V. We determined V_T by using a linear extrapolation of the linear portion of the $I_{DS} - V_{GS}$ curve at low drain voltages. The operating voltage for the devices is 1V. The simulation study has been conducted in two dimensions, hence all the results are in the units of per unit channel width.

The simulation of the device is performed by using Santaurus design suite [31, 32] with drift-diffusion, density gradient quantum correction and advanced physical model being turned on.

4. RESULTS AND DISCUSSION

In this section, computation of gate tunneling currents for a n-channel fully depleted nanoscale MOSFET through different stacked high-k dielectric structures have been carried out. This model calculates the gate tunneling current with energy loss (E_{loss}) during inelastic trap assisted tunneling process and $\alpha_{(chlov)}$ as fitting parameters. It is also assumed in our calculation that N_{trap}(x, E) is a

constant irrespective of position and energy level. Thus, present model is applicable to many alternate stacked high-k nano MOSFET structure simply by adjusting the two fitting parameter. The variation of total gate tunneling current with gate bias for a given values of EOT has been presented for possible alternative stacked gate dielectrics such as poly $Si/Si_3N_4/SiO_2/Si$, poly $Si/Al_2O_3/SiO_2/Si$ and poly $Si/HfO_2/SiO_2/Si$. The impact of inter layer dielectric thickness, type of gate stack and reverse gate stack on gate tunneling current as a function of gate voltages is reported in results for a given equivalent oxide thickness (EOT) of 1.0 nm with a 0.5 nm EOT for oxide and 0.5 EOT for high-k gate dielectric.

The comparision between the simulated data and the model value for gate tunneling current through different gate stack such as poly $Si/HfO_2/SiO_2/Si$, poly $Si/Al_2O_3/SiO_2/Si$ and poly $Si/Si_3N_4/SiO_2/Si$ is presented in Fig.3. The model value shows good agreement with the simulated value certifying the high accuracy of the propsed analytical modeling. This may be due to the fact that the possibility of carrier tunneling directly from channel to gate is low at large physical thickness of gate insulator (high-k gate dielectric) for a given equivalent oxide thickness (EOT).

For poly $Si/HfO_2/SiO_2/Si$ stack, simulation was carried out with t_{Hf02} = 2.82 nm, ϕ_{b_hk} (HfO_2) = 1.5 ev [35], m_{hk} = 0.18 m_o [35], $\sigma_t = 9.3 \times 10^{-16}$ cm^2 [36], $N_{trap} = 7.67 \times 10^{12}$ cm^{-2} [36]. The trap position (x_t) is extracted to be $0.37t_{Hf02}$ in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 2.82 nm. The fitting parameters E_{loss}, $\alpha_{(ch)}$ and $\alpha_{(ov)}$ has been taken to 0.4 eV, 0.72 and 0.47 respectively to fit the model with the simulated value. For poly $Si/Al_2O_3/SiO_2/Si$ stack, the simulation was carried out with t_{Al2o3} = 1.15 nm, ϕ_{b_hk} (Al_2O_3) = 2.8 ev [35], m_{hk} = 0.30 m_o [35], $\sigma_t = 7.03 \times 10^{-17}$ cm^2 [37], $N_{trap} = 2.4 \times 10^{12}$ cm^{-2} [37]. The trap position (x_t) is extracted to be $0.33t_{Al2O3}$ in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 1.15 nm. The fitting parameters E_{loss}, $\alpha_{(ch)}$ and $\alpha_{(ov)}$ has been taken to

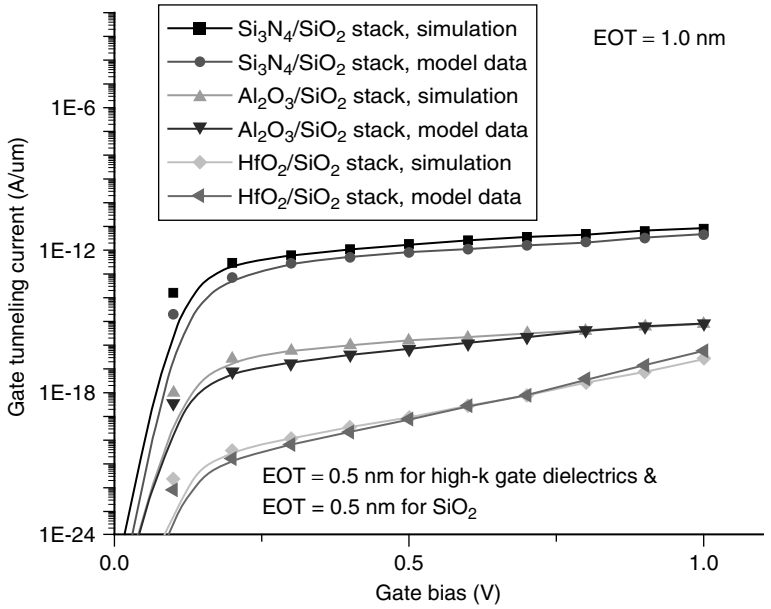

Figure 3. Comparison of analytical model data with Santaurus simulated data for different gate stack viz: poly $Si/Si_3N_4/SiO_2/Si$, poly $Si/Al_2O_3/SiO_2/Si$ and poly $Si/HfO_2/SiO_2/Si$ with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

0.7 eV, 0.8 and 0.57 respectively to fit the model with the simulated value. For poly $Si/Si_3N_4/SiO_2/Si$ stack the simulation was carried out with $t_{Si3N4} = 0.96$ nm, $\phi_{b\_hk}(Si_3N_4) = 2.0$ ev [35], $m_{hk} = 0.20\ m_o$ [35], $\sigma_t = 3 \times 10^{-13}$ cm^2 [38–39], $N_{trap} = 3 \times 10^{11}$cm^{-2} [40–41]. The trap position (x_t) is extracted to be 0.38 t_{Si3N4} in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 1.92 nm. The fitting parameters E_{loss}, $\alpha_{(ch)}$ and $\alpha_{(ov)}$ has been taken to 0.29 eV, 0.65 and 0.52 respectively to fit the model with the simulated value.

The high-k gate stack structure consisiting of poly $Si/HfO_2/SiO_2/Si$ is taken as an example to analyse the gate tunneling current behaviour with different thickness of inter oxide layer for same EOT of 1.0 nm in this work. The gate tunneling current for different inter oxide layer thickness is illustrated in the Fig. 4 to show the effects of inter oxide layer thickness. In this case, the gate tunneling current is reduced with increasing thickness of the inter oxide layer for the same EOT. This may be due to the fact that decrease in inter oxide layer thickness translates to increases in physical thickness of high-k dielectric layer. This increased physical thickness of high-k, in turn, lowers the vertical field responsible for carrier tunneling and reduces the gate tunneling current. However, it is also noted that the effect of gate current reduction with inter oxide layer cannot be generalized since the magnitude of gate current in high-k stack structures with inter oxide layer also depends on the interplay between other factors such as the barrier height, electron effective masses, as well as dielectric constant of the individual layers.

Fig. 5 plots the gate tunneling current vs gate bias with and without inter oxide layer i.e. for individual HfO_2 gate dielectric and HfO_2/SiO_2 gate stack respectively at an EOT of 1.0 nm. It is observed that gate tunneling current reduces to large extent for high-k gate stack as compared to individual high-k gate dielectric for same EOT. This may be due to the large interface barrier encountered by the tunneling electron when oxide layer is incorporated between high-k layer and substrate Si.

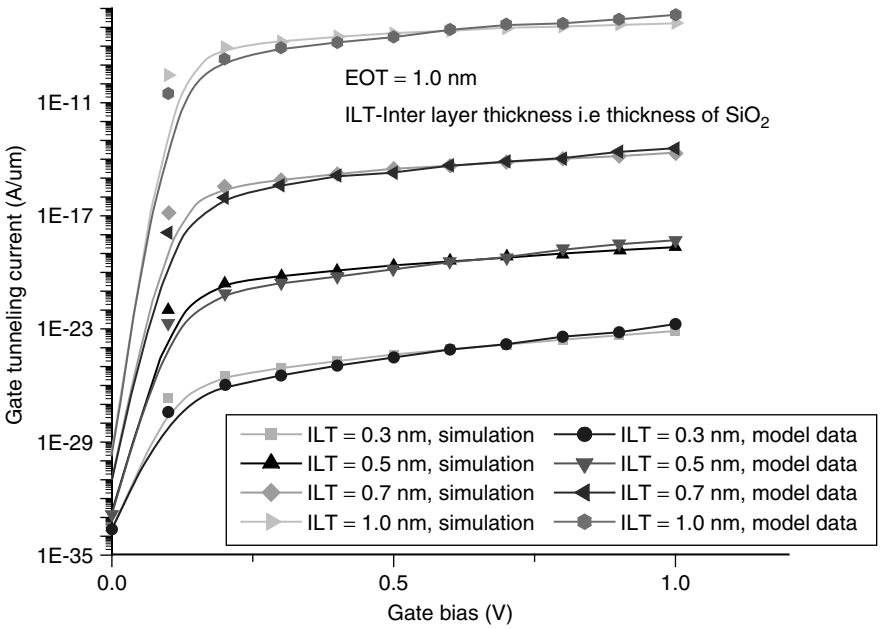

Figure 4. Gate tunneling current vs gate bias with inter layer thickness of oxide layer bas a parameter poly $Si/HfO_2/SiO_2/Si$ stack with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of $L_{met} = 25$ nm and S/D overlap length of $L_{ov} = 5$ nm in nano scale regime.

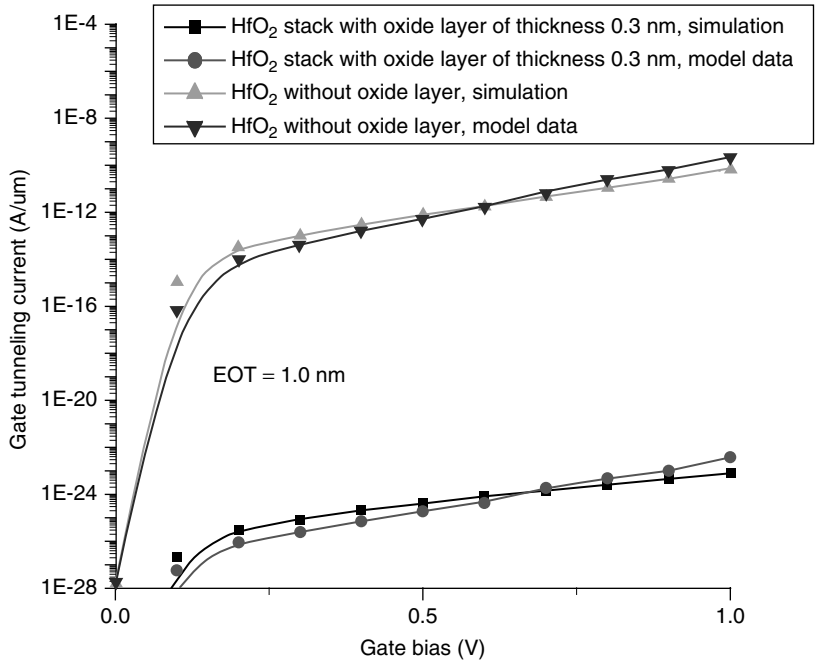

Figure 5. Gate tunneling current vs gate bias with and without oxide layer for HfO_2 gate dielectric at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

Fig. 6 presents the variation of gate tunneling current with gate bias for standard gate gate stack (Poly Si/HfO_2/SiO_2/Si) and reverse gate stack (Poly Si/SiO_2/HfO_2/Si) at a same EOT of 1.0 nm. It is shown in Fig. 6 that tunneling of carrier is more in case of reverse stack due to lower interface barrier encountered in case of reverse gate stack. It is , therefore, advisable to use the standard high-k gate stack with regard to gate leakage application.

Another important issue is the effect of introduction of high-k gate stack structure on off current and on current of the device. It is observed in Fig. 7 that on current improves with the introduction of high-k gate stack as compared to individual high-k gate dielectric. For high-k gate stack structure, reduced coupling of fringing field with channel lowers the inter carrier scattering in channel thereby enhancing the carrier mobility and on current.

The plot shown in Fig. 8 presents the effect of gate dielectric material on off current of the device. The off current improves for high-k gate stack structure in comparison to individual high-k gate dielectric as illustrated in Fig. 8. Since threshold voltage deceases with increase in fringing field coupling with channel carrier, so, introduction of high-k gate stack structure slightly increases the threshold voltage due to lower fringing field coupling with carrier. This, in turn, reduces the subthreshhold leakage thereby improving the off current of the device.

Fig. 9 represents the variation of DIBL(drain induced barrier lowering) with gate dielectric material of the device to show the effect of gate dielectric material on DIBL. It is observed that DIBL improves marginally for high-k gate stack in comparison to individual high-k gate dielectric due to decreased effect of fringing field through high-k gate stack structure.

The effect of gate dielectric material on SS of the device is plotted in Fig. 10, showing that SS of the device, also, improves slightly for high-k gate stack structure since the lateral electric field responsible for SS does not strongly depends on fringing coupling with carrier.

Thus, halo implanted nano scale MOSFET having high-k gate stack structure with smallest inter oxide layer and oxide spacer provides a lowest gate leakage along with a improved other characteristics of the device such as DIBL,SS , on current and off current

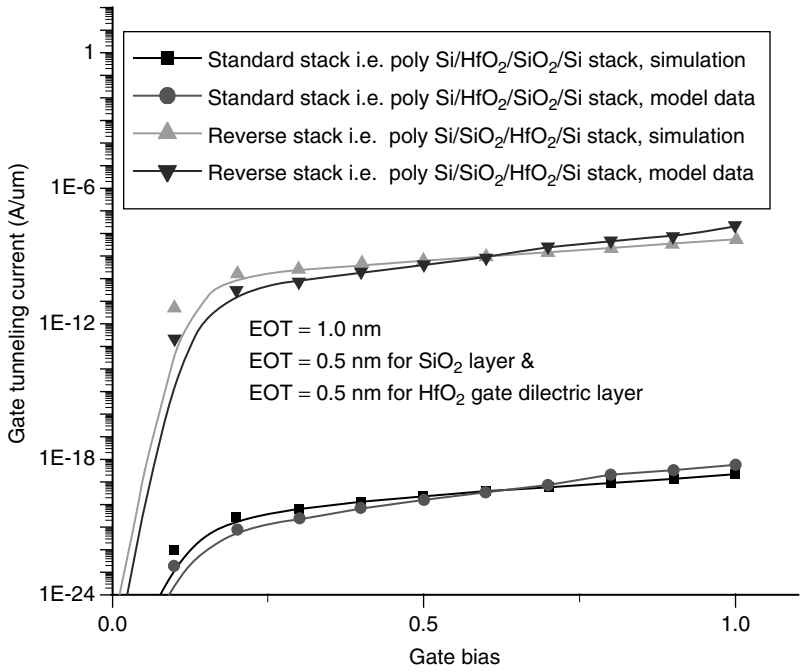

Figure 6. Gate tunneling current vs gate bias for standard gate stack i.e. poly Si/HfO_2/SiO_2/Si and reverse gate stack i.e. poly Si/SiO_2/HfO_2/Si at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

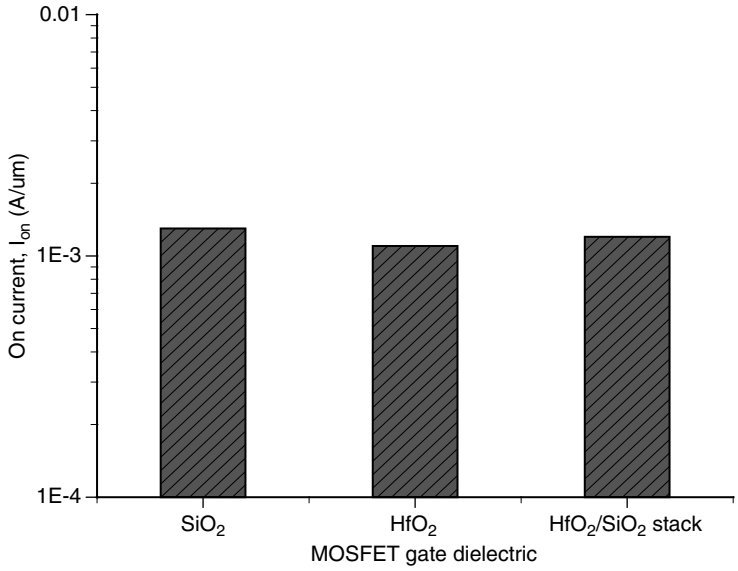

Figure 7. On current vs different gate dielectric such as only SiO_2, individual HfO_2 and poly Si/SiO_2/HfO_2/Si standard gate stack at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

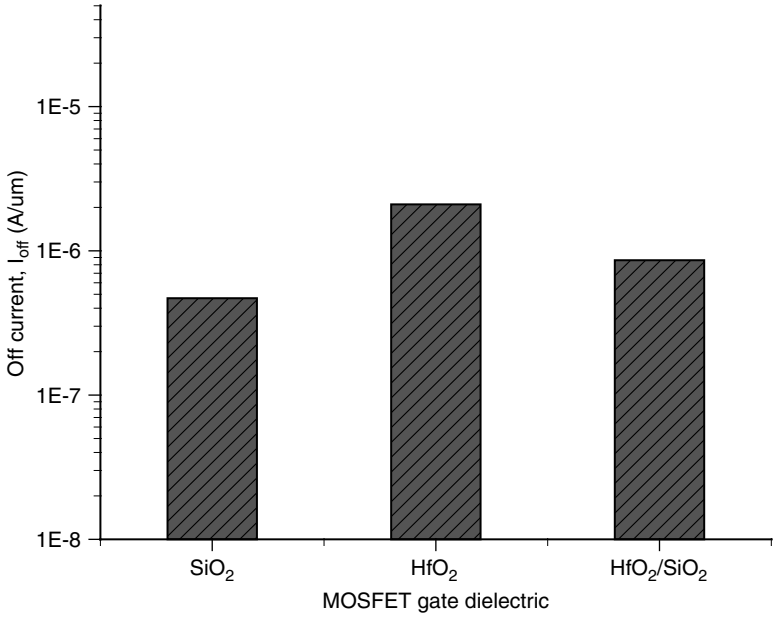

Figure 8. Off current vs different gate dielectric such as only SiO_2, individual HfO_2 and poly Si/SiO_2/HfO_2/Si gate stack at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

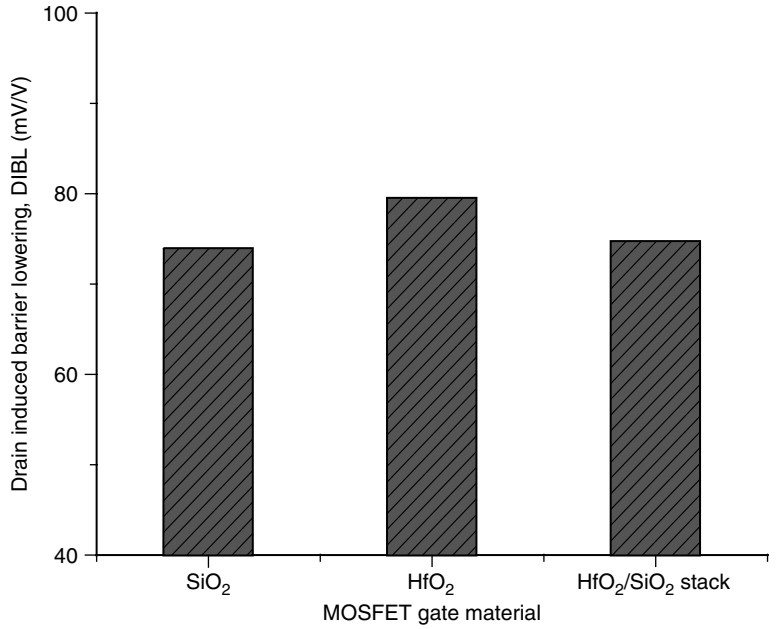

Figure 9. DIBL vs different gate dielectric such as only SiO_2, individual HfO_2 and poly Si/SiO_2/HfO_2/Si gate stack at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

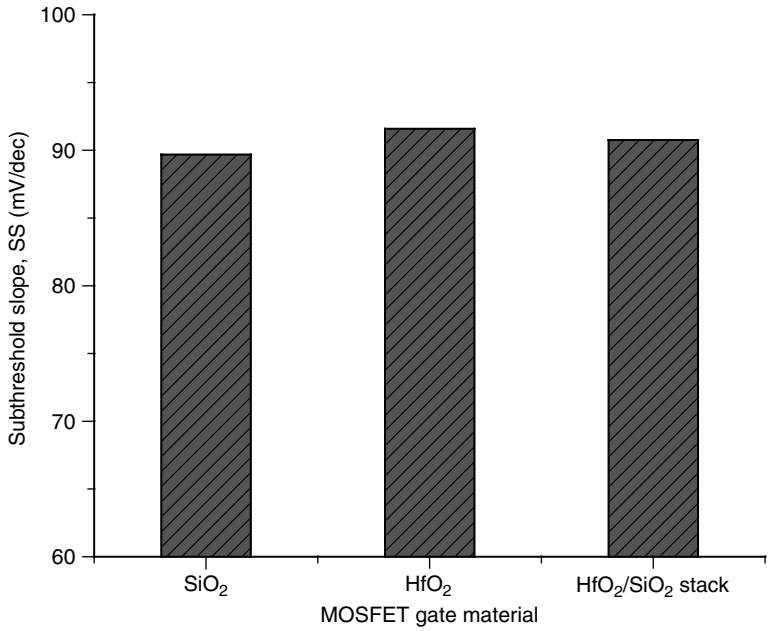

Figure 10. SS vs different gate dielectric such as only SiO_2, individual HfO_2 and poly Si/SiO_2/HfO_2/Si gate stack at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met} = 25 nm and S/D overlap length of L_{ov} = 5 nm in nano scale regime.

5. CONCLUSION

In this work, we have developed a simplified and compact analytical gate current model for nano scale N-MOSFET having high-k gate stack structure such as poly Si/Si_3N_4/SiO_2/Si, poly Si/Al_2O_3/SiO_2/Si and poly Si/HfO_2/SiO_2/Si. It is observed that results are in good agreement with the Santaurus simulated results. The present model has the following features as being conceptually simple, numerically efficient and especially applicable to various high-k stack structures consisting of combination of different dielectric materials and thickness, as well as for reverse gate stack structure simply by adjusting two fitting parameters. The introduction of high-k gate stack structure reduces the gate leakage to large extent as compared to individual high-k gate dielectric and improves the other characteristics of the device such as on current, off current, DIBL and SS.

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